REMARKS

Summary Of The Office Action & Formalities

Claims 1-5 are all the claims pending in the application. By this Amendment, Applicant is adding new claims 6 and 7. No new matter is added.

The Examiner has withdrawn the previous prior art rejections in view of Applicant's Response of November 13, 2003. However, the Examiner now rejects claims 1-5 under 35 U.S.C. § 103(a) as being unpatentable over Wong in view of newly cited Watanbe (USP 5,802,049).

Applicant respectfully traverses.

Claim Rejections - 35 U.S.C. § 103

1. Claims 1-5 In View Of Wong And Watanabe.

In rejecting claims 1-5 in view of Wong and Watanabe, the grounds of rejection state:

> Regarding claim 1, Wong teaches devices for switching ATM cells (figures 1-4; primary reference is made to the general architecture of figure 1 which figures 2- 4 are based upon) establishing a single path per virtual circuit having N.R inputs (k.n inputs) and N.R outputs (1.p outputs), N and R (k or 1, and n or p) being two integers not less than two, the device comprising at least two stages, including an inlet stage (n x m stage) comprising a plurality of matrices (1 to k) and having R.N sets (n.k sets) of Q outputs (r) and an outlet stage (s x p stage) comprising a plurality of matrices (1 to *l*) and having R.N sets (p.1 sets) of Q' inputs (r) - wherein n=p, m=n, and m=s (see page 709, col. 1, lines 4 and 17) and wherein figures 1 and 2 indicate k=l, thus n=m=s=p=R and k=1=N. Furthermore, the above is characterized in that for the flow of data carried by any intermediate link (one of the links in a grouping of r links, see page 708, column 2) that is part of the single path set up between an input and an output (r) to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input (n) of the inlet stage (n x m stage)

> can be connected to an output of the inlet stage (at m, one of the lines of a corresponding grouping of r lines) which can be selected only from Q outputs (r lines) associated with that input (e.g., r lines are provided "for each path between the two stages"); and in that each output (p) of the outlet stage (s x p stage) can be connected to an input of the outlet stage (at s, one of the lines of a corresponding grouping of r lines) which can be selected only from Q' inputs (r lines) of the output stage associated with that output (p). However, Wong may not specifically disclose an exclusive association between each inlet stage input/outlet stage output and each set of Q outputs/Q' inputs (r lines) such that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage.
>
> Watanabe teaches an improvement in ATM cell switching and, specifically, teaches an exclusive association between each of an inlet stage (e.g., secondary SRM 121-123 in FIG. 1) input and outlet stage (e.g., cubic SRM 131-133) output such that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage. Further, while Watanabe may disclose a preferred embodiment (e.g., FIG. 1) wherein a primary SRM stage (e.g., primary SRM 111- 113) may not also have the above-mentioned association (i.e., may not have cell copying functionality), Watanabe additionally contemplates an embodiment with such association by disclosing that the primary SRMs only "*normally* do not have the function of copying a cell" in order to "prevent the plurality of cells from the single cell in a single root from being output finally to the same leaf" [emphasis added] (e.g., see col. 3, lines 17-23). The teachings of Watanabe provide routing with high probability of success, reducing the lost-call rate when new subscribers are added for a point-to-multipoint connection (e.g., see col. 2, lines 26-38). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Watanabe to the system of Wong in order to provide reduce the lost-call rate when new subscribers are added for a point-to-multipoint connection.

Office Action at pages 2-4. Applicant respectfully disagrees.

Indeed, the current grounds of rejection, although applying a new reference, still do not meet the basic criterion set forth in the Manual Of Patent Examining Procedure ("MPEP") for

establishing a prima facie case of obviousness. In particular, the current grounds of rejection do not establish that there is some suggestion or motivation, either in Wong et al. or Watanabe to modify the switching architecture of Wong et al. so as to obtain Applicant's invention. Furthermore, the current grounds of rejection do not establish that the modification of the architecture of Wong et al. in view of Watanabe would include all the claim limitations. *See* MPEP §2142.

The Federal Circuit reminds us that the USPTO is held to a rigorous standard when trying to show that an invention would have been obvious in view of the combination of two or more references. *See, In re Lee*, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002), *citing, e.g., In re Dembiczak*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.").

The Federal Circuit goes on to emphasize that the "need for specificity pervades this authority." *In re Lee* at 1433 (emphasis added) (*citing In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed").

The current grounds of rejection fall short of the Federal Circuit's rigorous standard for demonstrating that the claimed invention would have been obvious. As explained below, Wong et al. and Watanabe, when considered together, do not provide the requisite suggestion or

motivation to modify the switching architecture disclosed in Wong et al. in order to obtain the claimed invention. Furthermore, these references do not teach or suggest all the claim limitations.

In rejecting claim 1, the grounds of rejection acknowledge that Wong et al. does not "disclose an exclusive association between each inlet stage input/outlet stage output and each set of Q outputs/Q' inputs (r lines) such that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage." Office Action at page 3.

Indeed, as Applicant has repeatedly argued, Wong et al. does not teach that "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input; and in that each output . . . of the outlet stage can be connected to an input of the outlet stage which can be selected only from Q' inputs . . . of the outlet stage exclusively associated with that output." That is, nowhere does Wong et al. teach or suggest the exclusive relationship recited in claim 1 between each input of the inlet stage and the associated Q outputs. Again, referring to Fig. 2 of the present application, for example, outputs $213_{1,1}$ through $213_{1,N}$ of the first inlet stage matrix 211_1 are exclusively associated with inputs 212_1. Similarly, outputs $213_{R,1}$ through $213_{R,N}$ of the first inlet stage matrix 211_1 are exclusively associated with inputs 212_R.

Newly cited Watanabe does not make up for the above deficiency. As with Cloonan et al., which was applied in the Examiner's previous rejection, Watanabe discloses a ***very particular*** switching architecture from input to output. The grounds of rejection have not pointed to any disclosure such that one skilled in the art would understand Watanabe to make the

sort of ***generalized*** teaching or suggestion argued in the grounds of rejection that could have motivated the skilled artisan to modify the switching network in Wong et al. Rather, given the technology and the ***infinite possible variations*** for modifying a switching network, the skilled artisan would require ***explicit instructions*** as to how to go about modifying the network in Wong et al. in the manner asserted in the grounds of rejection. Otherwise, when faced with these two disclosures, the skilled artisan is likely to entirely adopt ***one architecture or the other***, or engage in experimentation that could lead to any one of an infinite number of architectures.

Moreover, for the reasons repeatedly set forth by the Applicant in previous responses, Wong et al. would have ***taught away*** from Applicant's claimed invention, such that any experimentation, even in view of newly cited Watanabe, would lead the skilled artisan away from making the significant modifications needed to achieve the claimed invention. Claim 1 recites that the device for switching is "further configured so that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage." Wong et al. clearly does not teach or suggest this feature. To the contrary, referring to Fig. 1 of the reference, if one assumes, for the sake of argument, that for a given first stage (n x m) matrix each input is exclusively associated with a particular group r of outputs, then clearly each of these inputs is not associated with each second stage (s x p) matrix. The opposite is in fact illustrated in Fig. 1 of Wong et al. The grounds of rejection do not address this disclosure that teaches away from Applicant's claimed invention. *See, e.g., In re Hedges*, 228 USPQ 685, 687 (Fed. Cir. 1986) (describing how prior art references may "teach away" from a claimed invention, and concluding that teaching away provides "strong evidence of unobviousness").

Watanabe does not provide any direction to the skilled artisan to reject this feature of Wong et al. That is, the applied art provides no instruction on which features in Wong et al. and Watanabe to reject and which to maintain, let alone how to combine features from these two references.

The requisite teaching or suggestion for lifting certain features from one switching architecture and incorporating them into another switching architecture so as to achieve Applicant's claimed invention is simply not found in the applied art. Only when one skilled in the art relies on improper hindsight using Applicant's own disclosure as a road map can the skilled artisan reconstruct Applicant's invention.

Moreover, even if, ***for the sake of argument alone***, one skilled in the art were to modify the switching architecture of Wong et al. in view of Watanabe, the resulting structure would not include all the features of Applicant's claims.

Consider the fact that the first stage (i.e., inlet stage or primary SRM) clearly does not have the matrix architecture in which "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input . . . ." To the contrary, while Watanabe does not disclose the details of the input matrix architecture, it would appear that either each input of a ***primary*** SRM matrix is connected to a single output of that matrix, or that each input of a primary SRM matrix is connected to each output of that matrix. Neither case meets the requirement of claim 1.

Indeed, the grounds of rejection point to the architecture of the ***second*** stage (or secondary SRM) and then take the following two positions: (1) the secondary SRM discloses a

matrix architecture in which "each input . . . of the inlet stage can be connected to an output of the inlet stage which can be selected only from Q outputs . . . exclusively associated with that input . . . ." and (2) Watanabe teaches that the architecture of the secondary SRM can be used for the primary SRM. Applicant disagrees with both positions.

First, the grounds of rejection gloss over the fact that Watanabe explicitly ***teaches away*** from adopting the architecture of the secondary SRM for that of the first SRM "[t]o prevent the plurality of cells copied from the single cell in single root from being output finally to the same leaf . . . ." Watanabe at column 3, lines 20-22. Rather than reading the disclosure as one skilled in the art would, the grounds of rejection hinge on the word "normally" to draw an inference that is quite contrary to the actual disclosure.[1]

Second, even if, for the sake of argument alone, one were to modify the primary SRM matrices to have the architecture of the secondary SRM matrices, one would still not arrive at the relationship recited in claim 1. According to the architecture of a matrix in the secondary SRM, "copies from an input cell [are made] to a plurality of cells to be transmitted to a plurality of output paths." Watanabe at column 3, lines 17-20. Referring to Fig. 1 of the reference, the top matrix of the secondary SRM is illustrated as having an input that is connected by phantom lines to each of the outputs of that stage. Aside from that, the figure makes no further disclosure about the architecture. However, when one reviews Fig. 1 in view of the disclosure at column 3 noted

[1] Moreover, the suppositions set forth in the grounds of rejection are further alienated from any actual teaching or suggestion when one also keeps in mind that, according to the grounds of rejection, the alleged ***modified*** architecture of Watanabe would need to be used to further ***modify*** the architecture of Wong et al.

above, it is likely that each of the inputs to the top matrix in the secondary SRM is also connected to the same three outputs. Therefore, the secondary SRM matrices do not have an architecture that provides the exclusivity requirement recited in claim 1.

In summary, the grounds of rejection rely on multiple suppositions that are not rooted in the prior art and that do not meet the rigorous standard set forth by the Federal Circuit in *In re Lee.*

In view of at least the foregoing distinctions, the Examiner is kindly requested to reconsider and withdraw the rejection of claim 1 and dependent claims 2-5.

Additionally, regarding claims 2, 3, and 5, Applicant submits that the Examiner has not even established that the prior art recognizes any parameter as a result-effective variable, such that one skilled in the art would understand how to optimize the switching network. Indeed, the task facing the skilled artisan is not one that merely involves scaling up or down a parameter. Rather, claim 5 is directed to a unique architecture involving unique switching relationships that are not taught or suggested in the prior art.

Finally, with respect to claim 4, the Examiner has not identified specific grounds for rejecting this claim.

New Claims

For additional claim coverage merited by the scope of the invention, Applicant is adding new claims 6 and 7, which are believed to be allowable at least by reason of their respective dependencies.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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